Critical Conduction Mode PFC IC
FA1A00N / FA1A01N

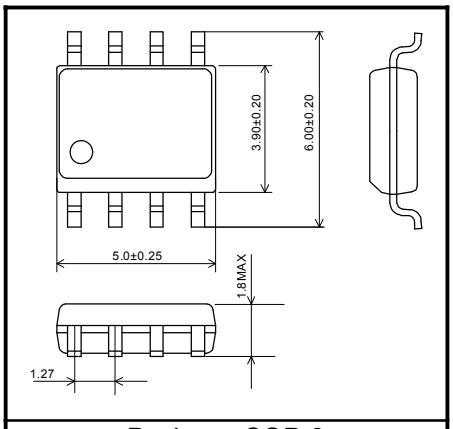
Datasheet

1. Overview

FA1A00/01 is power-factor correction converter IC operating in critical conduction mode. It realizes low power consumption by using high voltage CMOS process. It is equipped with many fault protection functions such as FB short-circuit detection circuit and double OVP function.

2. Features

- Very Low Standby Power by disusing Input Voltage Detection Resistors
- High-precision over current protection : 0.6V±2%
- Improved power efficiency at light load due to Maximum Frequency Limitation
- Soften Audible Noise at Startup
  Over Shoot Reduction functions
- Power factor improvement function
- Low current consumption by CMOS process
- Start-up : 500μA(typ.), Operating : 1.5mA(typ.)
- Enabled to drive power MOSFET directly
  Output peak current, source : 1000mA, sink : 1000mA
- Protects the output electrolytic capacitor by the double OVP function, even if a fault happen in the output detection.
- Open/short protection at feedback (FB) pin
- Protection circuit against short circuit of current detection resistor
- Under-voltage Lockout
- Restart timer
- 8-pin package (SOP)

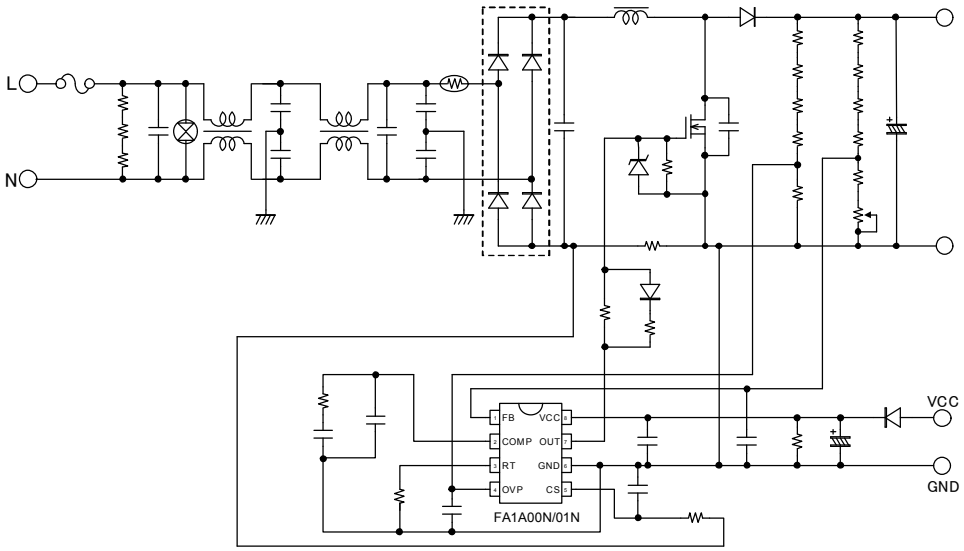


Package : SOP-8

3. Function list by types

Type	Startup Threshold	Double OVP function
FA1A00N	9.6V(typ.)	○
FA1A01N	12.4V(typ.)	○

4. Application circuit example



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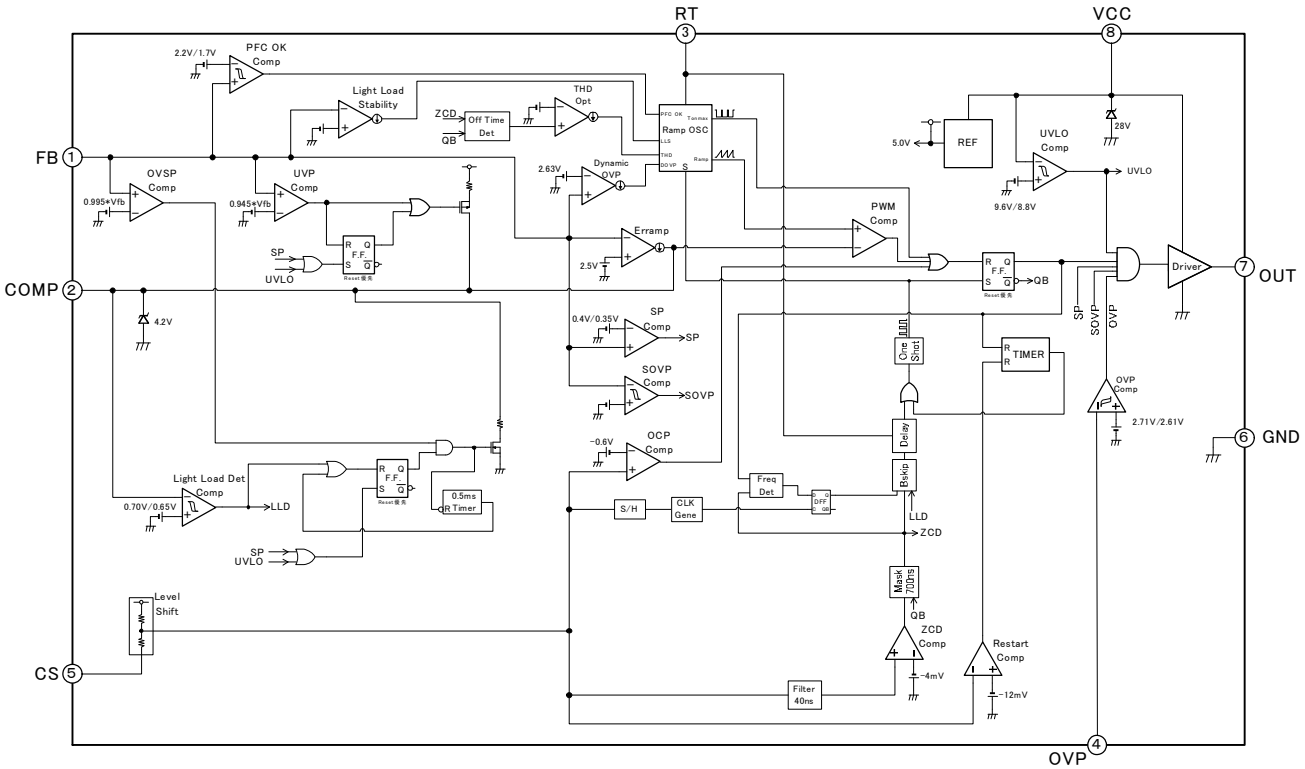
5. Block diagram

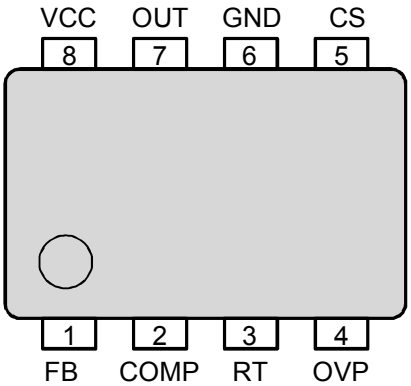
FA1A00N/FA1A01N



6. Functional description of pins

Pin No.	Pin name	Pin Function
1	FB	Feedback control signal input, Short Protection(SP), Dynamic Over Voltage Protection(DOVP), Static Over Voltage Protection(SOVP), Over Shoot Reduction *1
2	COMP	Error amplifier compensation, Light Load Stability *1
3	RT	Maximum on time and turn on delay setting
4	OVP	Over Voltage Protection(OVP) *1
5	CS	Current sense input, Frequency reduction, Power factor improvement, Over Current Protection(OCP) *1
6	GND	Ground
7	OUT	Output
8	VCC	Power supply, Under Voltage Lock Out(UVLO) *1

Notes)
*1 connect the capacitor.



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7. Rating & characteristics

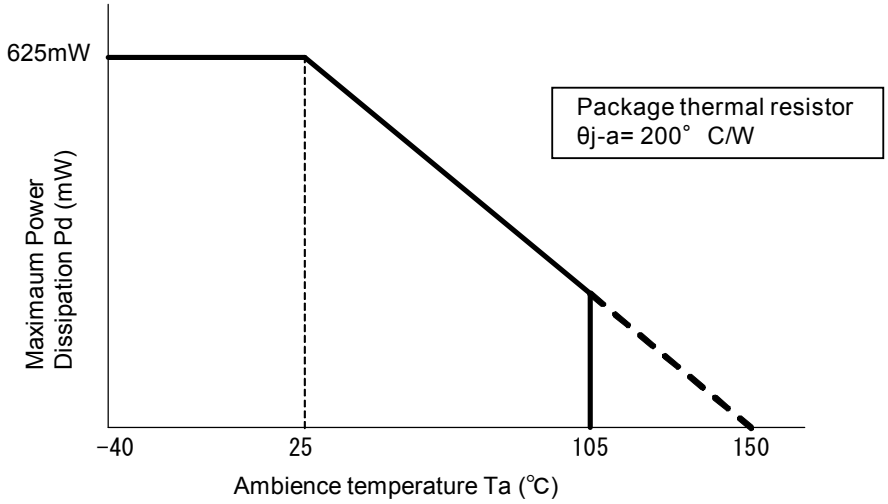
Stress exceeding absolute maximum ratings may malfunction or damage the device.
"-" shows source and "+" shows sink in current descriptions.

(1) Absolute maximum ratings

Item	Symbol	Value	Unit
Supply voltage	Vcc	28	V
Output peak current source or sink *2,*3	Io	-1000 +1000	mA
Voltage inputs(OUT)	Vinout	-0.3 to Vcc+0.3	V
Voltage inputs (FB,COMP,RT,OVP)	Vinfb,Vincomp, Vinrt,Vinovp	-0.3 to 5	V
Voltage inputs (CS)	Vincs	-3.3 to 0.3	V
Voltage inputs(CS) at startup(< 20ms) dV/dt=-10V/100ns	Vincs_vin	-10 to 0.3	V
Current inputs (FB,COMP,RT,OVP,CS)	Iinfb,Iincomp, Iinrt,Iinovp,Iincs	±100	uA
Current inputs(CS) at startup(< 20ms) *2	Iincs_st	-20	mA
Power dissipation(Ta=25℃) *2	Pd	625	mW
Operating junction temperature	Tj	-40 to +150	℃
Storage temperature	Tstg	-40 to +150	℃

Notes)
*2: Please consider power supply voltage and load current well and use this IC within maximum temperature in operation. The IC may cross maximum power dissipation at normal operating condition by power supply voltage or load current within peak current absolute maximum rating value
*3: The period that exceeds 500mA must be 100ns or less.

※Maximum dissipation curve



(2) Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	10	12	26	V
VCC pin electrolytic capacitor	Cvcce	10	-	-	uF
VCC pin ceramic capacitor	Cvccc	0.1	-	-	uF
Timing resistance	Rrt	100	-	390	kΩ
RT pin capacitor	Crt	-	0(Fix)	-	uF
Feedback and over voltage detect resistance	Rfb,Rovp	-	-	8	MΩ
CS filter resistance	Rcsf	47	-	100	Ω
Operating ambient temperature	Ta	-40	-	+105	℃

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(3) DC electrical characteristics

The characteristics in this section are those in conditions as follows unless otherwise specified. The voltages described in the conditions are DC input, not AC input.
Vcc=12V、Vfb=2.4V, Vcomp=4.2V, Rrt=33kΩ, Vovp=0V, Vcs=+10mV, OUT pin open and Tj=25℃
Notes)
(1) The item which indicated "*1" are not 100% tested and guaranteed by design.
(2) "—" means that it is not guaranteed.
(3) "-" shows source current and "+" shows sink current in output characteristics.

7-3-1) Error amplifier (FB pin, COMP pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage feedback input threshold	Vfb		2.475	2.500	2.525	V
Line regulation	Regline	VCC=10V to 26V	-20	-10	0	mV
Temperature stability	VdT	Tj=-30 to 85℃	-	±0.5	-	mV/℃
Transconductance	Gm	VFB(DC)=2.45V,2.65V VCOMP(DC)=Vfb Gm=Icomp_2.65 -Icomp_2.45/(2.65-2.45)	40	80	120	umho
Output source current	Icompso	VFB(DC)=0→1V, Vcomp(DC)=Vfb	-21	-13	-5	uA
Output sink current	Icompsi	VFB(DC)=4V VCOMP(DC)=Vfb	5	13	21	uA
FB pin threshold voltage when COMP pin pull up *2	Vfb_ comp_pull	VFB(DC) decrease	0.925 xVfb	0.945 xVfb	0.965 xVfb	V
COMP pull up resistance *2 when FB pin voltage decrease	Rcomp_ pull	VFB(DC)=2.0V VCOMP(DC)=1.0V	40	50	60	kΩ

*2 : FB pin voltage becomes "FB pin threshold voltage when COMP pin pull up" or less, COMP pin is pulled up by "COMP pull-up resistor when FB pin voltage decrease" (except at startup).

7-3-2) Ramp oscillator (RT pin, COMP pin, FB pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
OUT pin maximum on time (FB>PFC OK)	Tonmax	VFB(DC)=2.4V VCOMP(DC)=4.2V Toff(OUT)>Toffthd	10	14	18	us
OUT pin on time at THD optimize	Ton1	VCOMP(DC)=2V Toff(OUT)=10us	3	5	7	us
	Ton2	VCOMP(DC)=2V Toff(OUT)=2us	5	10	15	us
OUT pin off time THD optimize start *3	Toffthd	Ton(OUT)=Ton1x1.1	2	3	4	us
COMP pin threshold voltage for stop switching at OUT pin	Vthcomp	VCOMP(DC) decrease Switching at OUT pin stop	0.5	0.6	0.7	V
COMP pin clamp voltage	Vcomp _pull	VFB(DC)=1V	4.1	4.2	4.3	V
RT pin output voltage (FB>PFC OK)	Vrt	VFB(DC)=2.4V	2.6	2.8	3.0	V

*3: Off time of the OUT pin becomes "OUT pin off time THD optimize start" or less, on time of the OUT pin increase.

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7-3-3) PFC OK (RT pin, COMP pin, FB pin, CS pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
PFC OK FB pin threshold voltage *4	Vthfb_rth	VFB(DC) increase Ton(OUT) change	0.86 xVfb	0.88 xVfb	0.90 xVfb	V
	Vthfb_rtl	VFB(DC) decrease Ton(OUT) change	0.66 xVfb	0.68 xVfb	0.70 xVfb	V
OUT pin maximum on time when FB pin voltage decrease (FB<PFC OK) *5	Tonmax_rtl	VFB(DC)=1V	24	32	40	us
Detect delay of zero current when FB pin voltage decrease (FB<PFC OK) *5	Tzcd_rtl	VFB(DC)=1V	4	6	8	us
RT pin output voltage when FB pin voltage decrease (FB<PFC OK) *4	Vrt_fbl	VFB(DC)=1V	0	0	0.1	V

*4: FB pin voltage becomes “PFC OK FB pin threshold voltage” or less, RT pin voltage becomes “RT pin output voltage when FB pin voltage decrease”.
*5: FB pin voltage becomes “PFC OK FB pin threshold voltage” or less, on time of OUT pin and detect delay of zero current is determined by internal current of IC.

7-3-4) Over voltage comparator (FB pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Static OVP threshold voltage	Vsovph	VFB(DC) increase Switching at OUT pin stop	1.060 xVfb	1.080 xVfb	1.095 xVfb	V
	Vsovpl	VFB(DC) decrease Switching at OUT pin start	1.020 xVfb	1.040 xVfb	1.060 xVfb	V
	Vsovphys	Vsovph – Vsovpl	0.030 xVfb	0.040 xVfb	0.060 xVfb	V
Dynamic OVP threshold voltage	Vdovp	VFB(DC) increase Ton=Tonmax x0.7	1.025 xVfb	1.050 xVfb	1.075 xVfb	V

7-3-5) Over voltage comparator (OVP pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
OVP Pin OVP threshold voltage	Vovph	VOVP(DC) increase Switching at OUT pin stop	1.060 xVfb	1.080 xVfb	1.095 xVfb	V
	Vovpl	VOVP(DC) decrease Switching at OUT pin start	1.020 xVfb	1.040 xVfb	1.060 xVfb	V
	Vovphys	Vovph – Vovpl	0.030 xVfb	0.040 xVfb	0.060 xVfb	V

7-3-6) FB short comparator (FB pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
FB pin threshold voltage	Vthfbh	VFB(DC) increase Switching at OUT pin start	0.36	0.40	0.44	V
	Vthfbl	VFB(DC) decrease Switching at OUT pin stop	0.31	0.35	0.39	V

7-3-7) Light load stability function (COMP pin, RT pin))

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
COMP pin voltage when light load stability function start *6	Vthcomp_lls	Slope=Slp_rp1 x1.1	1.1	1.4	1.7	V
Ramp slope of light load stability function *6	Slp_rp1	VCOMP(DC)=2V (2-Vthcomp)/Ton(OUT)	0.15	0.25	0.35	V/us
	Slp_rp2	VCOMP(DC)=1.3V (2-Vthcomp)/Ton(OUT)	0.5	0.6	0.7	V/us

*6: COMP pin voltage becomes “COMP pin voltage when light load stability function start” or less, slope of ramp oscillation waveform becomes steep.

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7-3-8) Current sense comparator (CS pin, COMP pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CS pin threshold voltage	Vthcsh	VCS(pulse): High=10mV Low decrease dV/dT= ±40V/us	-612	-600	-588	mV
Temperature stability of CS pin threshold *1	Vthcshdt	Tj=-30 to 85℃	-1.5	-	+1.5	%
Delay to output	Tphl	VCS(pulse): High=10mV Low= -700mV dV/dT= -40V/us VOUT open	50	200	500	ns
Detect voltage of zero current	Vzcd	VCS(DC) increase	-7	-4	-1	mV
Detect delay of zero current	Tzcd	VCS(PULSE): High=10mV Low= -100mV dV/dT= +40V/us VOUT open	0.45	0.9	1.35	us
Masking time of zero current detect after OUT pin turn off	Tmask_ zcd	VCS(DC)=10mV Toff(OUT)-Tzcd	0.3	0.7	1.1	us
Detect delay of zero current	Ics	VCS=0V	-10.0	-7.0	-4.0	uA

7-3-9) Frequency reduction (CS pin, RT pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency reduction bottom 1 to 2 transition switching period *7	Tonoff12	VCS(PULSE) frequency increase OUT pin turn on timing change 1st ZCD to 2nd ZCD	5.6	6.6	7.6	us
Frequency reduction bottom 2 to1 transition switching period *1 *7	Tonoff21	VCS(PULSE) frequency increase OUT pin turn on timing change 2nd ZCD to 1st ZCD	9.0	11.0	13.0	us
Frequency reduction bottom 2 to 3 transition switching period *1 *7	Tonoff23	VCS(PULSE) frequency increase OUT pin turn on timing change 2nd ZCD to 3rd ZCD	3.4	4.4	5.4	us
Frequency reduction bottom 3 to 2 transition switching period *1 *7	Tonoff32	VCS(PULSE) frequency increase OUT pin turn on timing change 3rd ZCD to 2nd ZCD	6.8	8.8	10.8	us
OUT pin turn on timer (Bottom 2) *1 *8	Tonbt2	VCS(PULSE) ZCD time of CS increase OUT pin turn on time from 1st ZCD (Bottom 2)	1.8	2.8	3.8	us
OUT pin turn on timer (Bottom 3) *1 *8	Tonbt3	VCS(PULSE) ZCD time of CS increase OUT pin turn on time from 1st ZCD (Bottom 3)	3.2	4.2	5.2	us
Frequency reduction switch CS pin threshold voltage *1 *9	Vthcs_lph	VCS(DC) increase	-70	-40	-10	mV
	Vthcs_lpl	VCS(DC) decrease	-150	-100	-50	mV
Bottom 3 operation COMP pin threshold voltage *10	Vcompb3h	VCOMP(DC) increase	0.6	0.7	0.8	V
	Vcompb3l	VCOMP(DC) decrease	0.60	0.65	0.70	V

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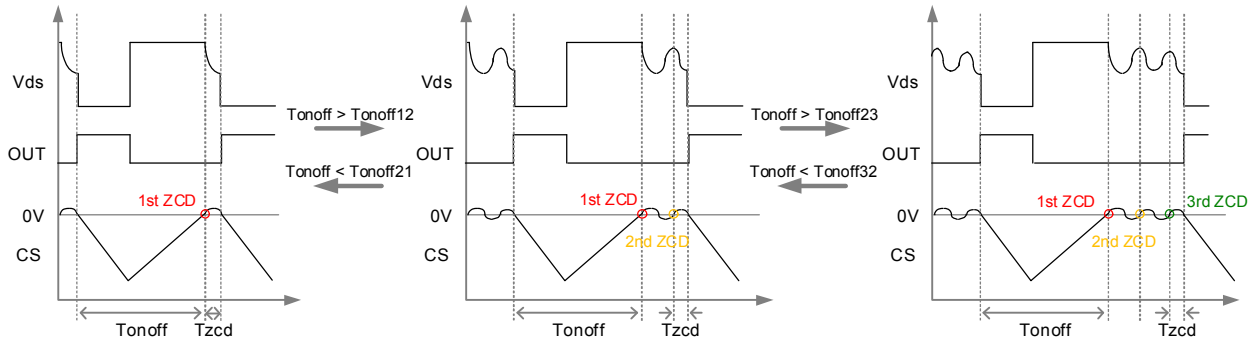
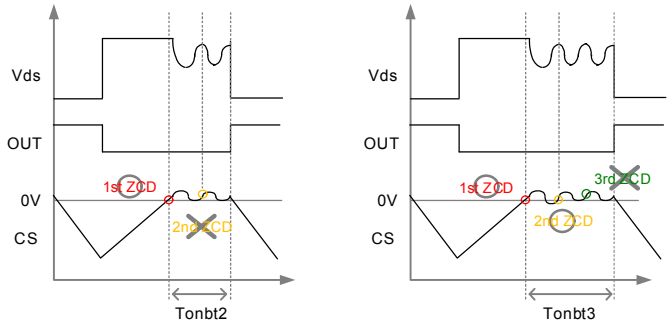
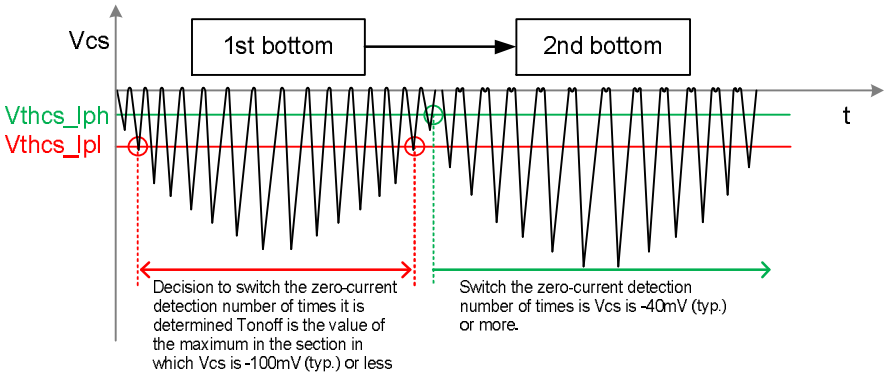
*7 : Switching period (From OUT pin turn on to zero current detection) becomes “Frequency reduction bottom transition switching period” or less, the number of zero current detection until OUT pin turn on increase



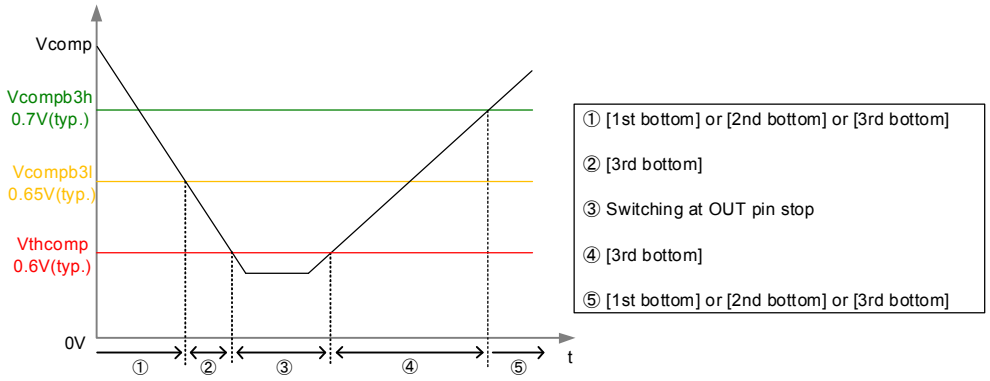
*8 : Period of zero current detection becomes longer than “OUT pin turn on timer (Bottom n)”, OUT pin turns on. When OUT pin turn on timer (Bottom) becomes longer than Restart timer delay, OUT pin turns on Restart timer delay.



*9 : Switching period becomes “Frequency reduction bottom transition switching period” or less, and CS pin voltage becomes “Frequency reduction switch CS pin threshold voltage” or more, then the bottom transition occurs.



*10 : COMP pin voltage becomes “Bottom 3 operation COMP pin threshold voltage” or less, the bottom 3 transition occurs.



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7-3-10) Over shoot reduction (FB pin, COMP pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
FB pin threshold voltage for over shoot reduction *11	Vthfbovs	VFB(DC) increase	0.96 xVfb	0.98 xVfb	0.995 xVfb	V
COMP pin pull down resistance at over shoot reduction *1 *11	Rcomp_ ovs	VFB(DC) increase	1.4	2	2.6	kΩ
Over shoot reduction operation period *1 *12	Tovs	VFB(DC) increase	0.2	0.5	0.8	ms
Over shoot reduction release COMP pin threshold voltage *12	Vcomp_ ovsh	VCOMP(DC) increase	0.6	0.7	0.8	V
	Vcomp_ ovsl	VCOMP(DC) decrease	0.60	0.65	0.70	V

*11: At startup, FB pin voltage becomes “FB pin threshold voltage for over shoot reduction” or more, COMP pin is pulled down by “COMP pin pull down resistance at over shoot reduction”.

*12: “Over shoot reduction operation period” has elapsed or COMP pin voltage becomes “Over shoot reduction release COMP pin threshold voltage”, pull down is released.

7-3-11) Driver output (OUT pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage low state	Vol1	VCOMP(DC)=0V Isink(OUT)=100mA	0.4	1.2	3.3	V
	Vol05	VCOMP(DC)=0V Isink(OUT)=50mA	0.2	0.6	1.5	
Output voltage high state *1	Voh1	Isouce(OUT)= -100mA	8	9	10	V
	Voh05	Isouce(OUT)= -50mA	9.5	10.5	11.5	
Output voltage rise time	Tr	C(OUT)=1000pF	20	100	300	ns
Output voltage fall time	Tf	C(OUT)=1000pF	10	50	250	ns

7-3-12) Restart timer(OUT pin, CS pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Restart timer delay (Normal operation)	Tdly_nor	VCS(DC)=Vthcs_rest	4	8	12	us
Restart timer delay (Protection)	Tdly_prot	VCS(DC)=200mV	100	200	300	us
CS threshold voltage at restart timer start	Vthcs_rest	VCS(DC) increase	-19	-12	-5	mV

7-3-13) Under voltage lock out (VCC Pin)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Startup threshold voltage	Von	Vcc increase Switching at OUT pin start	FA1A00N	8.6	9.6	10.6	V
			FA1A01N	11.4	12.4	13.4	V
Shutdown threshold voltage	Voff	Vcc decrease Switching at OUT pin stop	FA1A00N	7.8	8.8	9.8	V
			FA1A01N	7.8	8.8	9.8	V
UVLO hysteresis width	Vhysvcc	Von-Voff	FA1A00N	0.6	0.8	1.0	V
			FA1A01N	3.2	3.6	4.0	V

7-3-14) Power supply current (VCC Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Startup power supply current	Istart	VCC(DC)=Von-0.1V	300	500	700	uA
Operating power supply current	Icc	COUT=OPEN	0.3	1.5	3.0	mA
Dynamic operating power supply current	Iop	COUT=1000pF	0.5	2.0	4.0	mA
Stand-by current	Istb	VFB(DC)=0V VCOMP(DC)=0V	300	500	700	uA

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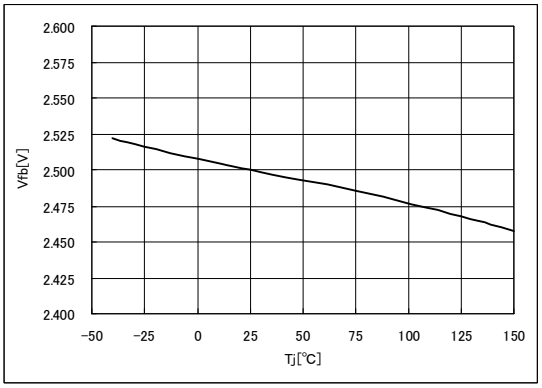
8. Characteristic curve

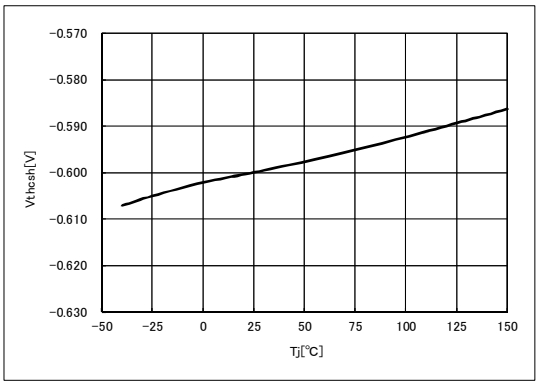
The characteristics in this section are those in conditions as follows unless otherwise specified.
Vcc=12V, Vfb = 2.4V, Vcomp=4.2V, Rrt= 160kΩ, Ovp=0V, Vcs = +10mV, OUT pin open and Tj = 25℃

Notes)
(1) ”-” shows source current and “+” shows sink current.
(2) The data listed here show the typical characteristics of an IC and it does not guarantee the characteristic.

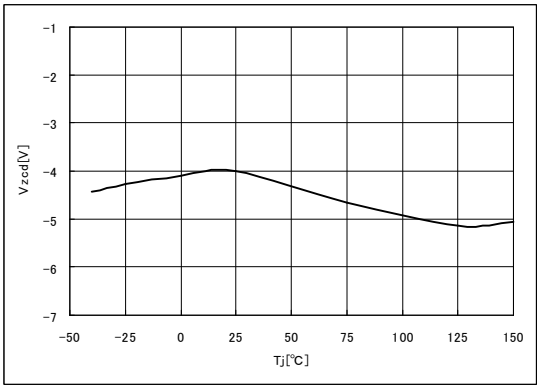
Voltage feedback input threshold(Vfb)
vs. Juntion temperature(Tj)



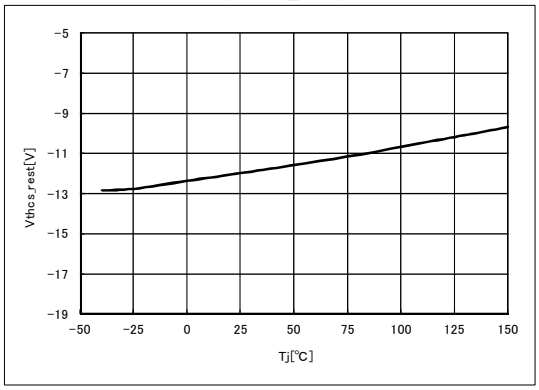
CS pin threshold voltage(Vthcsh)
vs. Juntion temperature(Tj)



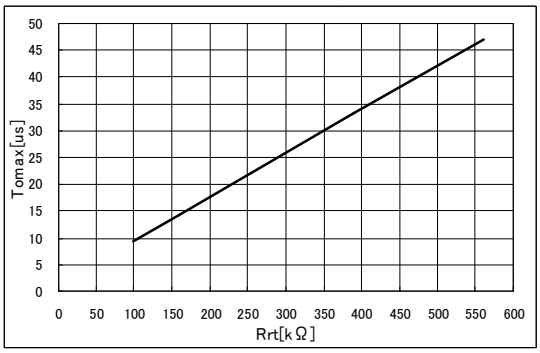
Detect voltage of zero current(Vzcd)
vs. Juntion temperature(Tj)



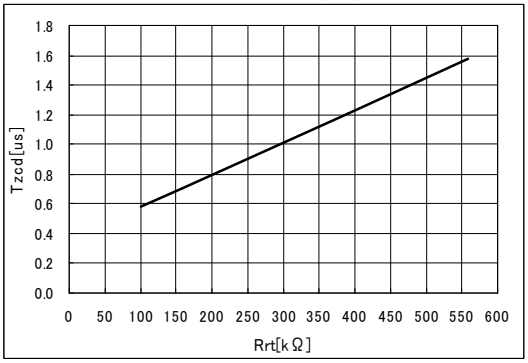
CS threshold voltage at restart timer
start(Vthcs_rest)



OUT pin maximum on time(Tonmax)
vs. RT resistance(Rrt)



Detect delay of zero current(Tzcd)
vs. RT resistance(Rrt)



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9. Outline of circuit operation

This IC is a power-factor correction converter utilizing a boosting chopper, operating in critical mode. Hereinafter is outline of the operation consisting of switching operation and power-factor correction operation using the circuit diagram shown in Fig. 1.

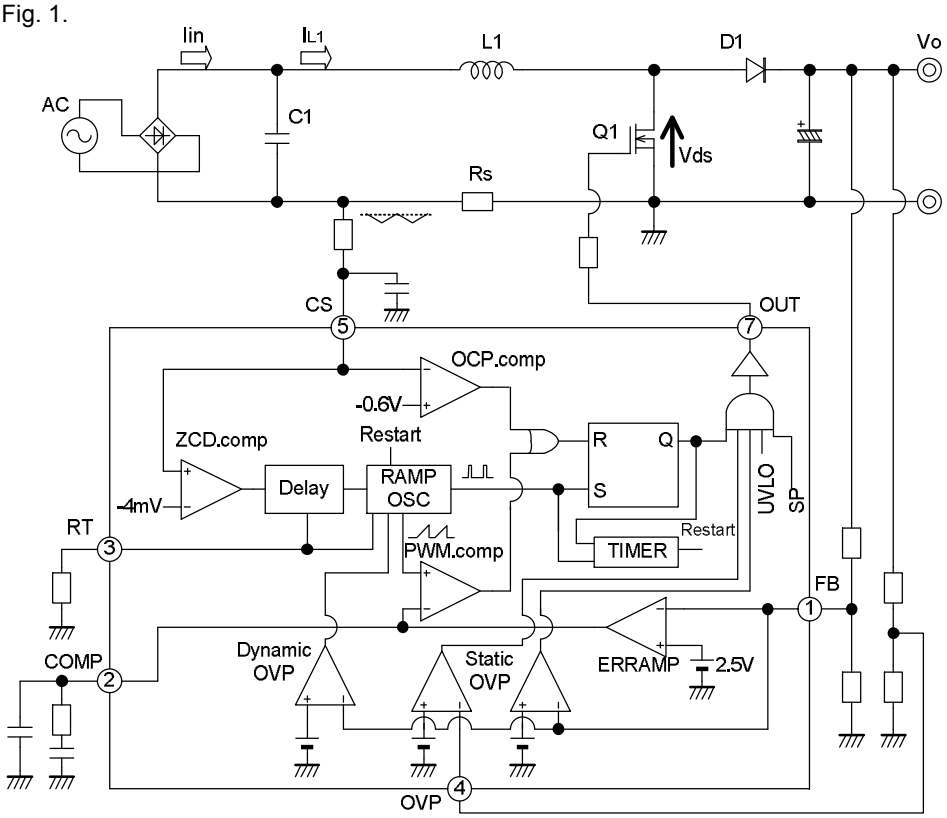

Fig.1 Block diagram of operating circuit

(1) Switching operation

This IC performs the switching operation in the critical mode applying self-oscillation without using an oscillator. Fig.2 shows the outline of waveforms of the switching operation in steady state. The operation is as follows.

【t1】Q1 turns on, the current through inductor (L1) rises from zero. At the timing of Q1 on, Vramp; output of ramp generator states to rise.

【t2】Vramp and Vcomp; output of the error amplifier are compared by the PWM comparator, and when Vramp>Vcomp, Q1 turns off and the output of the ramp generator drops.
When Q1 turns off, the voltage across L1 inverts and the current through L1 decreases while the current is supplied to the output side through D1.

【t3】The current through L1 is detected by Is terminal, and when the current becomes zero, the output of the current detection comparator becomes High to turn on Q1 after delay given by the delay circuit, thus moving to the next switching cycle (t1).

By repeating the operations of t1 ~ t3, the switching in critical mode is continued.

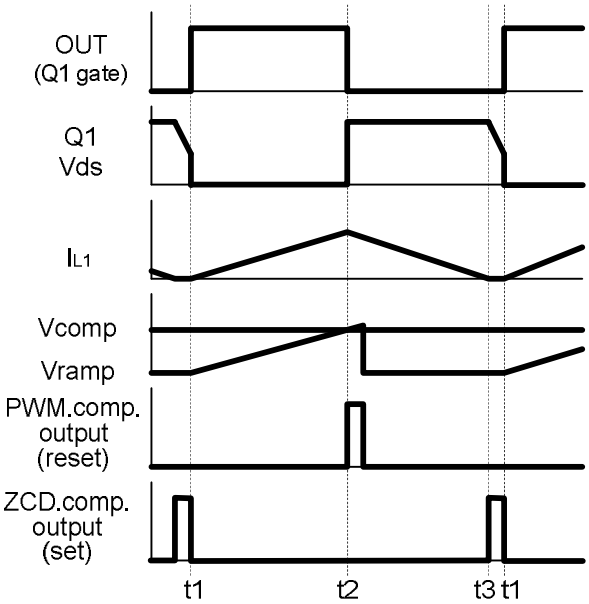

Fig. 2 Switching Operation, Waveforms

With the power-factor correction circuit in the critical mode, the switching frequency is always changing due to instantaneous values of the AC input voltage. The switching frequency also changes when the input voltage or load changes.

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(2)Power-factor correction operation

As explained in the switching operation, the current flowing through the inductor repeats in triangular waveforms.
The mean value (IL1(mean)) of the triangular wave current becomes 1/2 of the peak value (IL1(peak)). (Fig. 3)

By controlling to make outline linking the peak of the inductor current to sine wave and removing switching ripple current, the smoothed current flowing from the AC input power source has sine wave shape.

FA1A00/01 uses fixed on time control shown in Fig. 4.
This control determines the on time of the output of IC (gate drive signal for Power Mos) with combination of the error amplifier output and saw tooth wave. While the load is constant, the output of the error amplifier is constant, and on time also stays constant. Since an inclination of inductor current depends on input voltage (an inclination of inductor current is proportional to input voltage) and on time is constant, the outline linking the peak of the inductor current becomes same AC waveform as the input voltage, which enables power-factor correction operation.

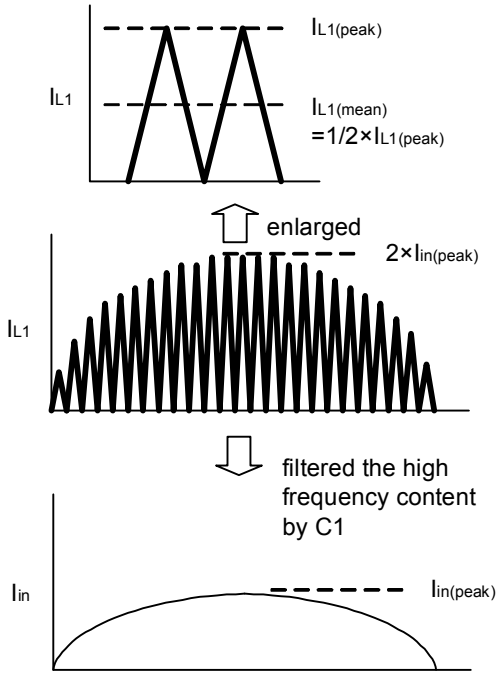

Fig.3 : Power-factor correction operation waveforms

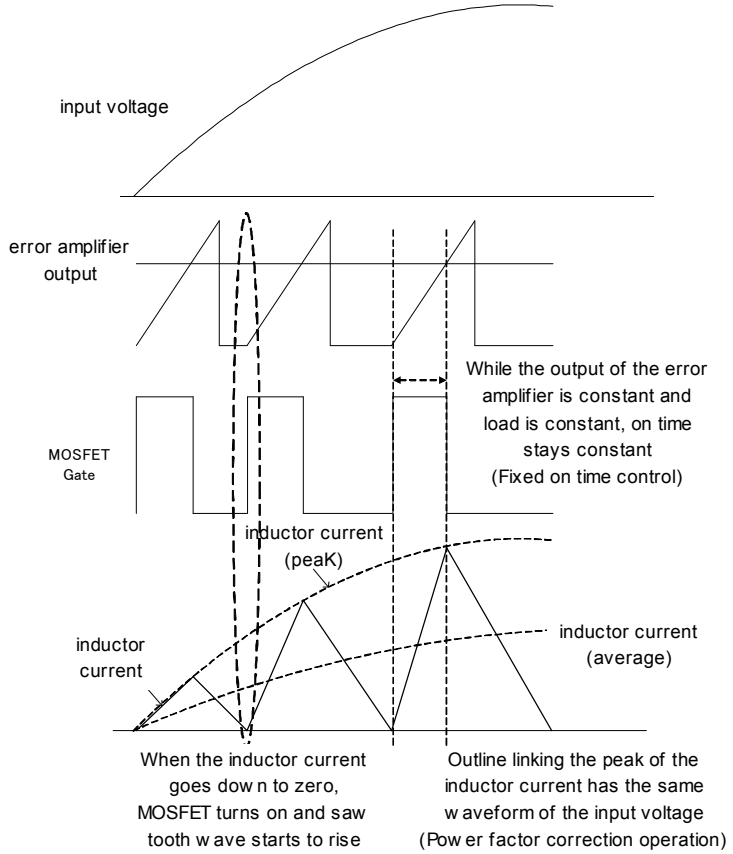

Fig.4 : Fixed on time control

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10. Description of each circuit block

(1) Error amplifier circuit

The error amplifier is to make the output voltage constant with feedback control. For this IC, a transconductance type is used for the error amplifier. The non-inverting input terminal is connected to internal reference voltage of 2.5V (typ.). The inverting input terminal is fed with output voltage of the power-factor correction converter, and normally use divided voltage with resistors. To the inverting input, internal constant current source of 1.8μA is connected for FB open detection function.
The output of the error amplifier (COMP) is connected to the PWM comparator and controls the on time of the OUT output.
The output voltage of PFC contains much of ripple of frequency 2 times AC power line (50 or 60Hz). When this ripple component becomes largely appears in the output of the error amplifier, the power-factor correction converter does not stably operate. In order to obtain the stable operation, connect capacitors and a resistor at Pin No. 2 (COMP) as shown in Fig.5.

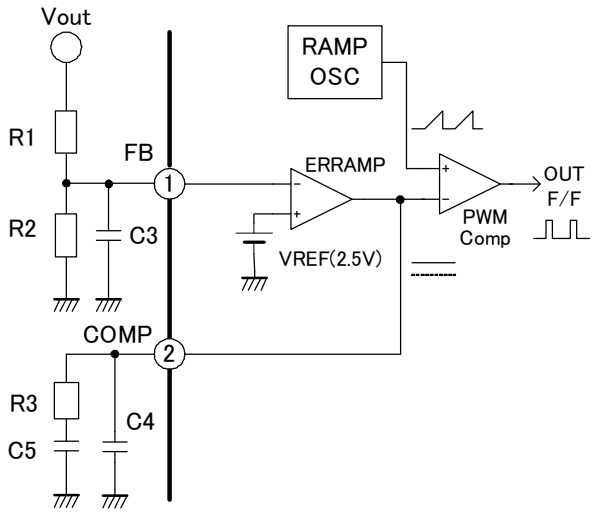

Fig.5 Error amplifier circuit

(2) Overshoot reduction circuit

To suppress the overshoot of output voltage at startup, the FA1A00/01 has an overshoot reduction function. If the voltage starts increasing after the UVLO or standby mode is reset, and reaches the overshoot reduction operation start FB voltage (0.98 x Vfb(typ.)), the overshoot reduction circuit pulls down the COMP pin voltage temporarily and limits the ON width of the OUT pin, thereby suppressing the increase in the output voltage and reducing overshoot (Fig. 6).
Once the overshoot reduction is actuated, it remains actuated unless it is reset by entering the UVLO or standby mode.

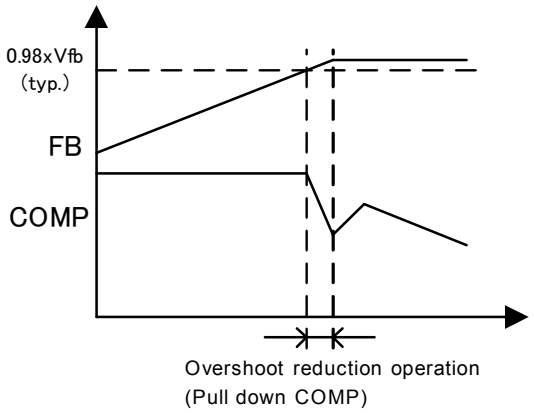

Fig.6 Overshoot reduction operation

(3) Overvoltage protection circuit (OVP)

This circuit is to limit the voltage when the output voltage of the power-factor correction converter exceeds the set value.
When this IC starts up or load changes sharply, the output voltage of the converter may exceed the set value. In such a case, this protection circuit works to control the output voltage.
FA1A00/01 has 2 of OVP function as shown below.

It controls the ON width linearly when the output exceeds the reference voltage.
Dynamic OVP - - - Built-in FB pin

It stops the output pulse when the output exceeds 1.08(typ.) times of reference voltage.
Static OVP - - - Built-in FB pin and OVP pin

The operation of FB pin which has two functions above is described below.

FB pin voltage is usually 2.5V as same as the reference voltage. When the startup or a sudden change of load, FB pin voltage rises and will exceed 2.5V. In this case, a function which limits ON width depending on FB pin voltage becomes active. (Dynamic OVP) If FB pin voltage rises more and exceeds a reference voltage of comparator (Vfb x 1.08(typ.)), another function becomes active and stops the output pulse during exceeding the reference. (Fig.7)
When FB pin voltage decreases to 1.040(typ.) times of reference voltage or lower, IC outputs pulses again.

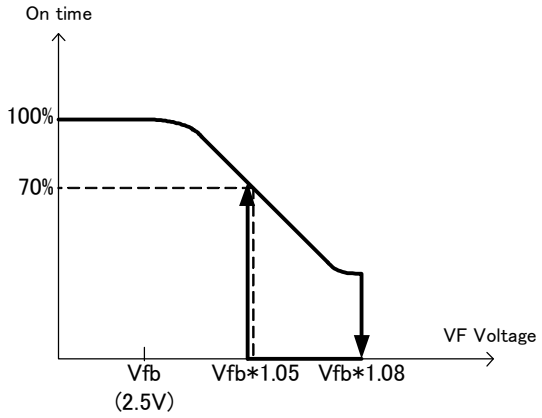

Fig.7 On time at overvoltage

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(4)FB short/open-circuit detection circuit

(Standby circuit)

In the PFC circuit of booster type, if feedback voltage is not properly provided to the FB pin due to short-circuit or open-circuit around R1, R2, the error amplifier cannot control the constant voltage and the output voltage abnormally rises. In such a case, the overvoltage protection circuit also cannot operate because the detection of the output voltage is abnormal. To avoid such situation, this IC is equipped with FB short-circuit detection circuit.

This circuit is composed of the reference voltage and comparator (SP), and when the input voltage of the FB pin becomes 0.35V(typ.) or lower due to such trouble as short-circuit of R2 or opening of R1, the output of the comparator (SP) inverts to stop the output of the IC and the IC stops operation resulting in standby state.

Once the voltage of the FB pin decreases to almost zero and the output of the IC stops, and then when the voltage of the FB pin returns to 0.4V(typ.) or higher, the IC resumes from the standby state and the OUT pulse restarts.

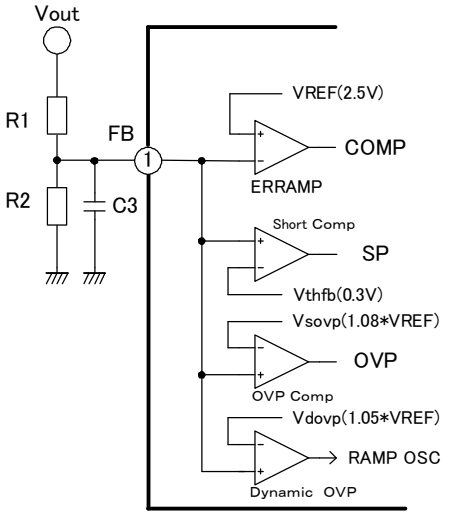

Fig.8 FB pin circuit

(5) Current detection circuit

The current detection circuit is composed of zero current detection and overcurrent detection. (Fig.9)

(5-1) Zero current detection circuit

This IC performs the switching operation by self-oscillation in critical mode instead of the oscillator with the fixed frequency. The zero current detection circuit ZCD. Comp detects that the inductor current becomes zero to perform the critical mode operation.

With the zero current detection, the voltage across the current detection resistor Rs connected to the GND line is fed to the CS pin, and it is compared by the zero current detection comparator, and when it becomes -4mV(typ.) or more, the inductor current is regarded as zero level.

When the zero level is detected, the delay Tzcd is generated by the zero cross delay detection circuit, and then set the F/F for OUT to make MOSFET turn on.

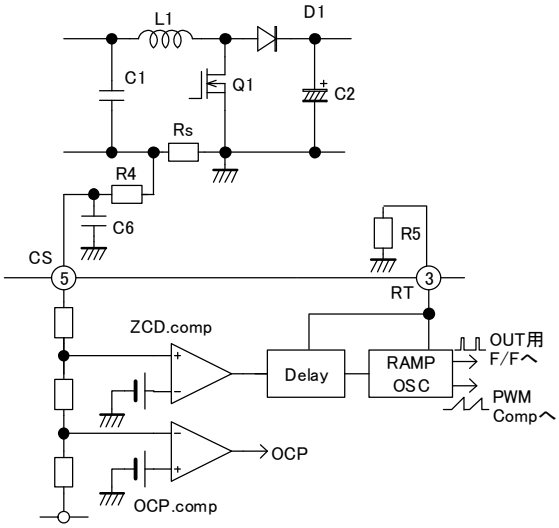

Fig.9 Current detection circuit

(5-2) Overcurrent detection protective circuit

The overcurrent detection protective circuit detects the inductor current and protects MOSFET by turning off the OUT output when it becomes higher than a set current level. With the overcurrent detection, the voltage across the current detection resistance Rs connected to the GND is fed to the CS pin, and when the CS pin voltage compared by the overcurrent detection comparator becomes lower than -0.6V(typ.), it is regarded as overcurrent state. When the overcurrent is detected, the F/F for OUT output is reset to make MOSFET turn off.

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(6) Zero cross delay time setting circuit

Vds between the drain and the sources of the MOSFET starts oscillating through resonance of L1 and the parasitic capacitor component on the circuit just before the MOSFET turns on.
When the proper value of Rrt, the turn on timing of MOSFET can be adjusted at the bottom of the voltage oscillation. This makes it possible to minimize the switching loss and the surge current generated at the turn-on. (Fig. 10)
When the Rrt is smaller, the turn-on timing becomes earlier, and vice versa. (Fig. 11)
Since the optimum value of this Rrt changes depending on the circuit and input/output conditions, tuning up is required so as to achieve an optimum state while evaluating the operation with actual circuit.

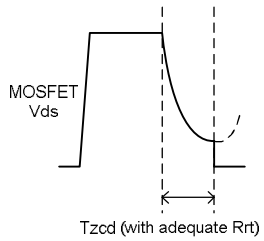

Fig.10 Vds waveform at turn on (with adequate Rrt)

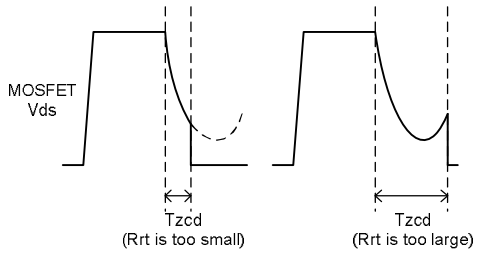

Fig.11 Vds waveform at turn on (with inadequate Rrt)

(7) Ramp oscillating circuit

The ramp oscillating circuit receives signal from the zero current detection circuit or restart circuit, and outputs the set signal of F/F for OUT output and saw tooth wave signal for deciding the duty of the PWM comparator.

(7-1) Frequency reduction function

The PFC in critical mode has characteristics that its switching frequency increases under light load.
FA1A00/01 has the frequency reduction function to increase the efficiency, and limit the increase in frequency, under light load.
The period from the time when the MOSFET is set to ON (High of OUT) to the time when zero current is detected by the CS pin (ON/OFF interval) is measured, and depending on the ON/OFF time, the MOSFET ON timing is determined.
If the ON/OFF interval is 11us or longer, the frequency reduction function is not actuated. As shown in Fig. 12, when zero current detection delay time Tzcd has elapsed after the zero level of the inductor current is detected, the MOSFET is turned on, thereby turning on Vds at the bottom

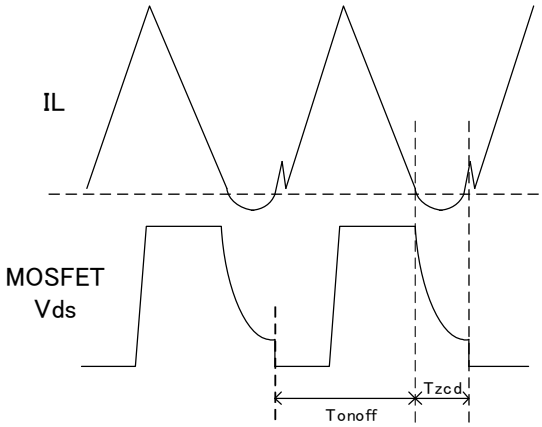

Fig.12 Waveform when the frequency reduction function is not operating. (at heavy loads)

<u>Frequency reduction function operating</u>

【1st bottom ⇒ 2nd bottom】
Tonoff < Tonoff12
Tonoff12: 6.6us(typ.)

【2nd bottom ⇒ 1st bottom】
Tonoff > Tonoff21
Tonoff21: 11us(typ.)

【2nd bottom ⇒ 3rd bottom】
Tonoff < Tonoff23
Tonoff23: 4.4us(typ.)

【3rd bottom ⇒ 2nd bottom】
Tonoff > Tonoff32
Tonoff32: 8.8us(typ.)

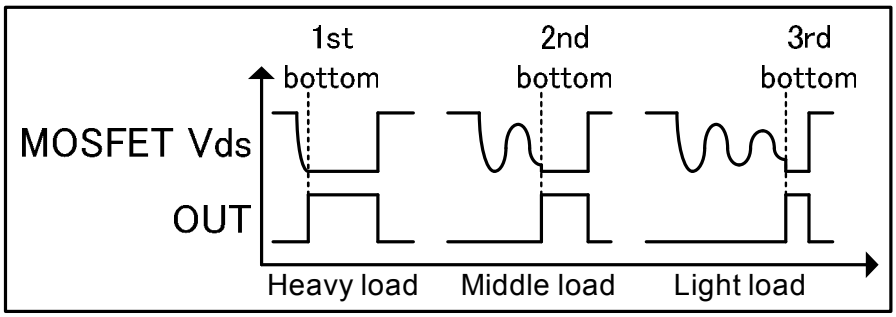

Fig.13 Waveform when the frequency reduction function is operating.

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(7-2)Power factor improvement function

Power factor decreases when inductance peak current is small, as when the phase angle of the input voltage is small, input voltage is high, and load is light. This IC has the function of detecting the MOSFET OFF period, increasing the ON width when the OFF period becomes correction start OFF width of 3us(typ.) or shorter, and increasing the peak current, thereby improving the power factor (Fig. 14).

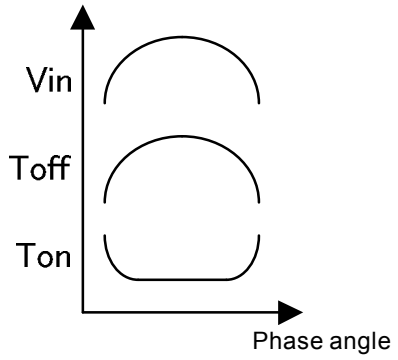

Fig.14 Power factor improvement function

(8) Restart timer

This IC utilizes self oscillation instead of the oscillator with fixed frequency, and in the steady operation, it turns on MOSFET with a signal from the zero current detector.
But in start up or light load condition, a trigger signal is required for starting up or stable operation.
This IC is equipped with a restart timer, and when a state where the OUT output of the IC is in Low output and the CS pin remains at -12 mV(typ.) or higher continues for 200us(typ.) or longer, an OUT signal is generated automatically. This signal can realize stable operation even when starting up or the load is light.

(9) Under voltage lock out (UVLO)

UVLO is equipped to prevent circuit malfunction when supply voltage drops. When the supply voltage rises from zero, the operation starts at 9.6V (typ.) for FA1A00 and 12.4V (typ.) for FA1A01.When the supply voltage decreases after the operation starts, either part number stops the operation at 8.8V (typ.).
When UVLO is on and IC stops operation the OUT terminal becomes LOW and cuts off the output. The current consumption of the IC decreases to 700uA(max) or less.

(10) Output circuit

The output portion is of push-pull circuit and can directly drive the MOSFET.
The peak current of the output portion is 1.0A maximum for sink and 1.0A maximum for source.

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11. How to use each pin and advice for designing

(1) Pin No.1 (FB pin)

Functions

(ⅰ) Input of feedback signal of output voltage setting
(ⅱ) Detect short-circuit of FB pin
(ⅲ) Detect output overvoltage

How to use

(ⅰ) Feedback signal input
- Connection method
  Connect the node between voltage dividing resistors for setting output voltage.

- Operation
  The output voltage Vout of PFC is controlled so that FB voltage matches the internal reference voltage (2.5V(typ.)).

$$Vout = \frac{VREF}{R2} \times R1 + VREF$$

VREF : Reference voltage = 2.5V (typ.)

For avoiding malfunction by noise, the recommended resistance of the detection circuit is 8Mohm or smaller.
To prevent malfunction due to noise, capacitor C3 of 1nF~47nF should be connected between the FB pin and GND.

(ⅱ) FB pin short-circuit detection
- Connection method
  Same as for the (ⅰ) Feedback signal input

- Operation
  When the input voltage of the FB pin becomes 0.35V(typ.) or lower due to short-circuit of R2, the output of the comparator (SP) inverts to stop the output of the IC.

(ⅲ) Output overvoltage detection
- Connection method
  Same as for the (ⅰ) Feedback signal input

- Operation
  Normally the voltage of the FB pin is 2.5V almost same as the reference voltage of the error amplifier. When the output voltage rises for some reason and the voltage of the FB pin reaches the comparator reference voltage (VREF x 1.09(typ.)), the output of the comparator (OVP) inverts to stop the OUT pulse. If the output voltage returns to the normal value, the OUT pulse resumes.

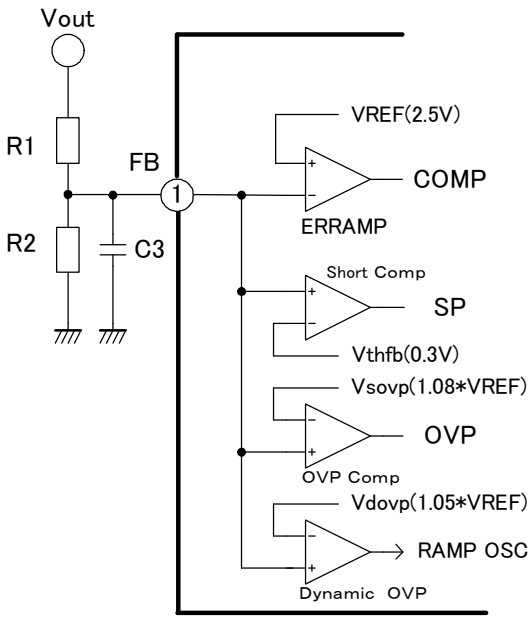

Fig.15 FB pin circuit

(2) Pin No.2 (COMP pin)

Functions

(ⅰ) Phase compensation of internal ERRAMP output

How to use

(ⅰ) Phase compensation of internal ERRAMP output
- Connection method
  Connect C, R between COMP pin and GND as shown in Fig. 16.

- Operation
  Connecting C, R to the COMP pin suppress ripple component at 2 times the frequency of the AC line that appears in the FB output.

(Reference)
Example of application circuit: C4=0.1uF
C5=0.47uF
R3=33kΩ
The above is a reference example, and it should be decided by sufficiently verifying with actual application circuit.

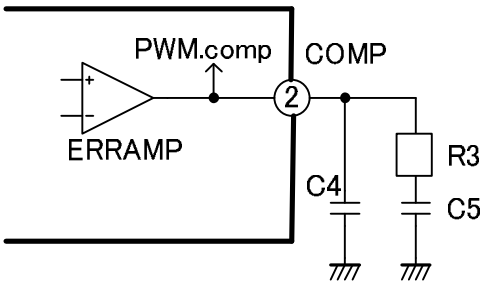

Fig.16 COMP pin circuit

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(3) Pin No.3 (RT pin)

Functions

(ｉ)Set maximum ON time
(ii)Set delay time for zero current detection

How to use

(ｉ)Set maximum ON time

ON time Ton in each switching cycle with input and output conditions is theoretically expressed by the following formula.

$$Ton = \frac{2 \times Lp \times Po}{Vac^2 \times \eta}$$

Input Voltage (Vrms): Vac
Inductor (H): Lp
Maximum Output Power (W): Po
Efficiency: η

The maximum ON time Tonmax must be set equal to or more than the ON time at minimum input voltage Vac (min) at which the ON time is maximum. The maximum ON time should be set as shown by the following formula.

$$Tonmax > \frac{2 \times Lp \times Po}{Vac(min)^2 \times \eta}$$

- Connection method

Connect R5 between RT and GND as shown in Fig. 17.
For the resistance dependency of the maximum ON time and maximum oscillation frequency, see Chapter 8. Characteristic Curve. The current sourced from the RT pin changes depending on the resistance connected.

(ii)Set delay time for zero current detection

Select a resistance value so that the delay time allows the MOSFET to be turned on when Vds hits the bottom (=approximately 0 V).
(See Section 10 (6) Zero cross delay time setting circuit.)
Adjustment is normally made based on high input state of the AC input range (around 240V AC when the voltage ranges from 90V to 264V AC). However, very smaller resistance makes maximum ON width Tonmax narrower and maximum output power fewer. Avoid choosing the resistance which gives narrower ON width than the result of above equation.
If the resistance gives much longer delay time, we recommend an adjustment of the delay time by the resonant capacitor.

【Additional explanation 1】

This IC has the frequency reduction function, and the bottom skip operation inhibits the switching frequency increase at light load, which is particular to the critical mode. Therefore, the input current waveform may be non-monotonic at the low input voltage (Fig. 20) and sound may be generated at the high input voltage depending on the constant of the RT pin resistance Rrt. Take the following countermeasures for solving this problem.

- Input current waveform at the low input voltage

  Increase the Rrt, widen the maximum ON width and change the operating point of the bottom to decrease the non-monotonic waveform.

- Sound generated at the high input voltage

  Decrease the Rrt, narrow the maximum ON width and increase the switching frequency.

In addition, the frequency reduction function uses the resonance phenomenon between the inductor and the capacitor on the circuit. When the MOSFET or diode is changed, it may be necessary to readjust the Rrt. If the Rrt is readjusted, reassess also the actual equipment.

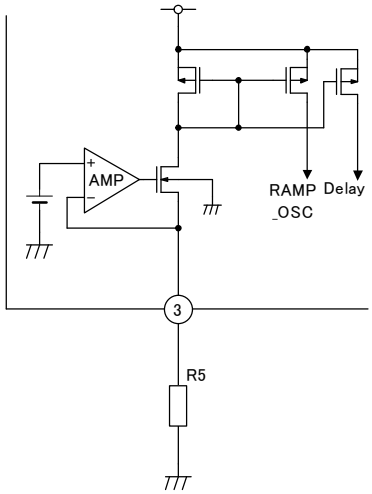

Fig.17 RT pin circuit

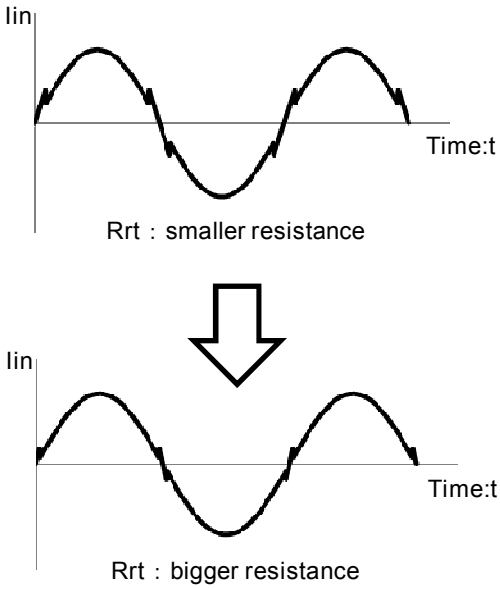

Fig.18 Input current waveform at the low input voltage

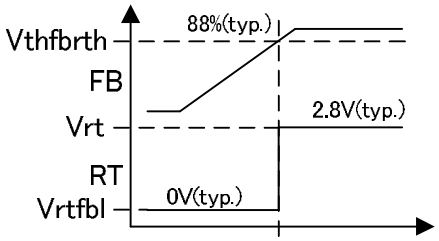

Fig.19 PFC OK at start-up

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【Additional explanation 2】

The FB terminal voltage is detected and the RT terminal output is kept at 0V (typ.) until the FB terminal voltage exceeds 88% (typ.) of the rated voltage 2.5V (typ.). When it exceeds 88% of the rated voltage, the RT terminal output is increased to 2.8V (typ.). When the RT terminal voltage is 0V (typ.), the turn-on delay time and the maximum ON width are fixed to 6us (typ.) and 32us (typ.), respectively, by the IC internal current regardless of the maximum ON width and turn-on delay time preset by the RT terminal resistance. (Fig. 19)

(4) Pin No.4 (OVP pin)

Functions

(ⅰ)Set detection level of OVP

It sets a voltage which detects an over voltage of output and which stop switching operation.

For avoiding malfunction by noise, the recommended resistance of the detection circuit is 8Mohm or smaller.

$$R8 = \frac{Vstop \times R9}{Vref \times 1.095}$$

Vstop: Overvoltage detection voltage,
Vref: OVP Reference voltage =2.5V)
1.095: Vovp Max(1.095xVref)

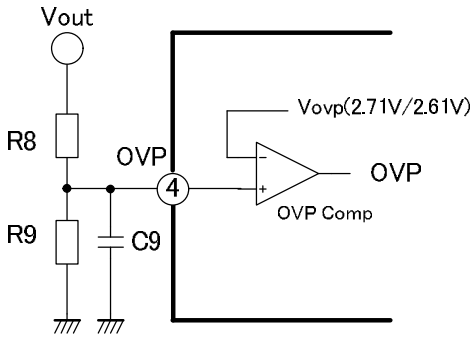

Fig.20 OVP pin circuit

(5) Pin No.5 (CS pin)

Functions

(ⅰ)Detect zero current through the inductor

(ⅱ)Detect overcurrent and turn off OUT output

How to use

The maximum threshold voltage Vthcsh of the CS pin is -0.588V(max).

The current detection resistance Rs is set so that necessary current can be supplied for this Vthcsh.

With maximum output Po (W) and minimum input voltage Vac (min), the maximum value of peak current (ILP (max)) through the inductor can be approximately expressed by the following formula.

$$I_{LP(max)} = \frac{2 \times \sqrt{2} \times Po}{\eta \times Vac_{(min)}}$$

Therefore, the value of Rs (Ω) is determined as follows.

$$Rs < \frac{-V_{thcsh}}{I_{LP(max)}} = \frac{0.588}{I_{LP(max)}}$$

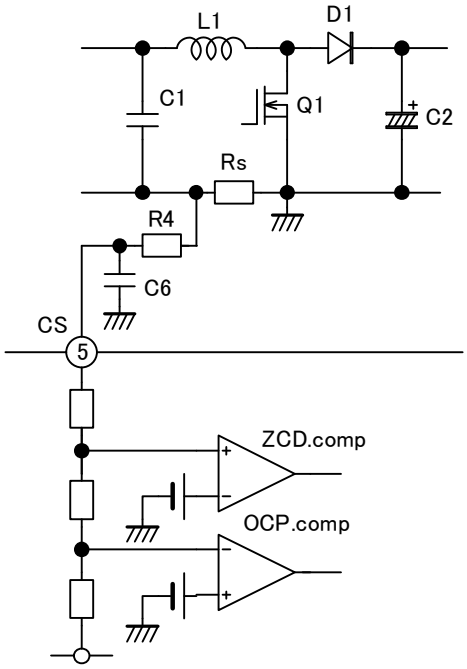

Fig.21 CS pin circuit

- Connection method

Connect the current detection resistor Rs between the source pin (GND) of MOSFET and the minus lead of the input capacitor (C1). The voltage across Rs is fed to the IC as the current/voltage conversion signal.(Fig.21)

- Operation

(ⅰ)Detect zero current through the inductor

The internal reference voltage and the internally divided voltage of the CS pin are inputted to the ZCD comparator, and when the IS pin voltage becomes larger than -10mV, the comparator output inverts and turns on the OUT output.

(ⅱ)Detect overcurrent and turn off OUT output

When the CS pin voltage becomes smaller than -0.6V, the comparator output signal inverts and turns off the OUT output.

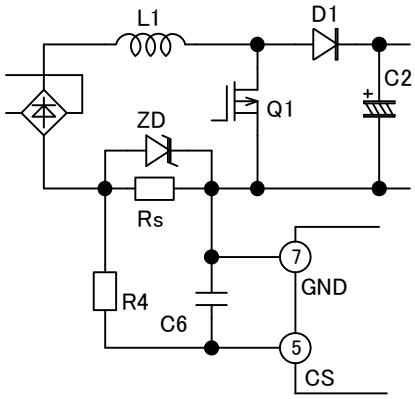

Fig.22 CS pin protection circuit (1)

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【Additional explanation】

When MOSFET turns on, the gate driving current of MOSFET and surge current due to discharging the parasitic capacitors run to the current detection resistance Rs. Large surge current may cause malfunction following disturbed input current waveform. Depending on the amperage of the surge current or timing, whisker-like pulse may be mixed in the turn-on portion of the OUT pulse of the IC. Normally, therefore, a CR filter is connected as shown in Fig.21. The cutoff frequency of this CR filter must be set sufficiently higher than the switching frequency so that it will not affect the normal operation.
It is recommended to set this cutoff frequency to about 1~2MHz.

$$\frac{1}{2\times\pi\times C6\times R4} \fallingdotseq 1 \text{ to } 2[\text{MHz}]$$

Since the threshold level is made through resistance dividing voltage as shown in Fig.21, the input resistor R4 is recommended to be 47Ω-100Ω.The voltage rating of the CS pin is -3.3V.
In case of an ordinary boosting circuit, rush current to charge the output smoothing capacitor C2 runs at the moment the ac input voltage is connected. This current may become far larger in comparison with the input current during normal operation.
As a result, far larger voltage may also be applied to the CS pin than the ordinary case.
In order to avoid damage, protective circuit must be taken in design so that voltage higher than -10V(< 20ms), absolute maximum rating, will not be applied to the CS pin even when such AC input voltage is connected. If voltage higher than the rating is predicted to be applied to the CS pin, use rush preventive circuit suppress rushing current or place Zener diode shown in Fig. 22 and Fig. 23.
In addition, for wiring to the CS pin, the wiring impedance must be small to decrease the influence of noise that may cause malfunction.

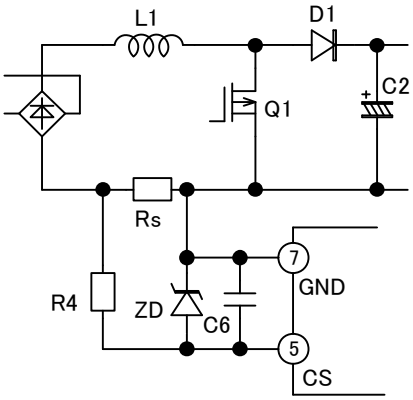

Fig.23 CS pin protection circuit (2)

(6) Pin No.6 (GND pin)

Function

This voltage of GND pin is the reference for each portion of whole circuits.

(7) Pin No.7 (OUTpin)

Function

This drives MOSFET.

How to use

- Connection method

Connect it to the gate pin of MOSFET through resistance.

- Operation

During the period when turn on MOSFET, the output state is high, and the output voltage is almost VCC.
During the period when turn off MOSFET, the output state is low, and the output voltage is almost 0V.

【Additional explanation】

The gate resistor is connected to limit the current of the OUT pin and prevent oscillation of the gate pin voltage. The rating of the output current is 1A for source and 1A for sink.
Using the connections shown in Fig. 25 and Fig. 26, it is possible to independently set the gate driving current of turning on and off MOSFET.

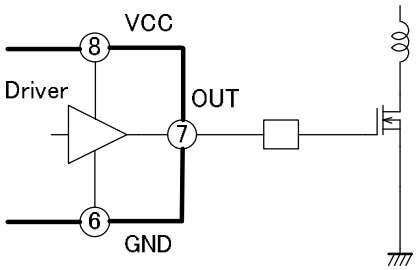

Fig.24 OUT pin circuit (1)

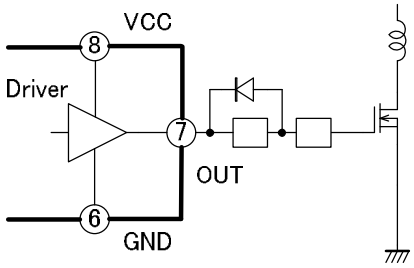

Fig.25 OUT pin circuit (2)

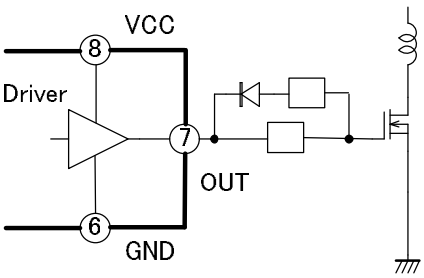

Fig.26 Out pin circuit (3)

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(8) Pin No. 8 (VCC pin)

Function

(i) Supply the power of IC.

How to use

(i) Supply the power of IC.

- Connection method

Connect the start up resistor R7 between VCC pin and Voltage line after rectifying from AC line, which supplies power before IC starts switching operation.
In general application, the power is provided from the auxiliary winding of the transformer through D2 during operation.
In some application, DC power supply can be connected.

- Operation

In the application without DC power supply to feed VCC terminal, the current through start up resistor R7 charges the smoothing capacitors C5 and C9, and when VCC voltage rises to the on threshold voltage of UVLO, the IC starts operating. Before starting operation, it is necessary to supply current higher than 80uA (max), the startup current of the IC. During steady operation, the VCC is supplied from the auxiliary winding of the inductor. (Fig. 27)
When the supply voltage rises from zero, the operation starts at 9.6V (typ.) for FA1A00 and 12.4V (typ.) for FA1A01.
If the supply voltage decreases after the operation starts, the operation stops at 9V (typ.) by UVLO for both ICs. After IC stops operation due to UVLO, the OUT terminal is Low state to cut off the output.

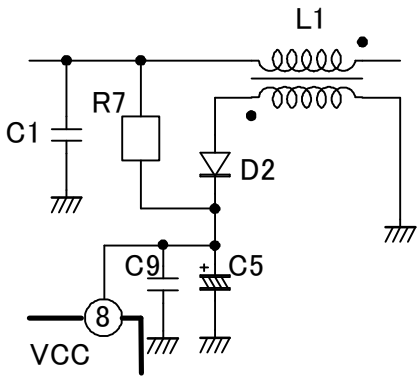

Fig.27 VCC pin circuit (1)

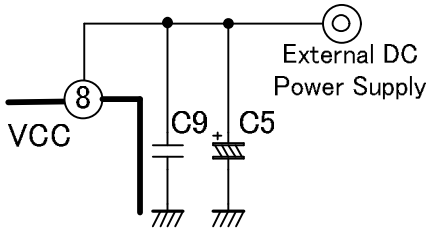

Fig.28 VCC pin circuit (2)

【Additional explanation】

UVLO is preventive function to keep the circuit from malfunction when the supply voltage decreases.
With the startup resistor R7, it is necessary to supply current of 700μA or higher, the startup current, until start operating, and the following formula must be satisfied.

$$R7 < \frac{\sqrt{2} \times Vac(min) - Von(max)}{700 \times 10^{-6}}$$

Von(max) : Startup threshold voltage :
FA1A00:10.6V(max)、FA1A01:13.4V(max)

The value of R7 expressed with the formula is, however, at least necessary and minimum condition to start the IC, and actually it should be decided considering the starting up time required for each application circuit.
This starting up time must be examined by measuring in actual circuit operation.

During the steady operation, Vcc is supplied from the auxiliary winding of the transformer. But there is some time delay until the auxiliary winding voltage sufficiently rises after the IC starts switching operation. To prevent Vcc from decreasing to the off threshold voltage of UVLO, it is necessary to decide the capacitance of the C5 connected to Vcc. Since this time delay differs depending on the circuit, it should be decided after checking with actual circuit
It is also recommended to place the ceramic capacitor C9 (about 0.1uF) to remove switching noise.

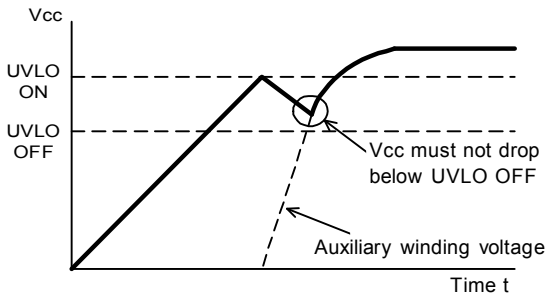

Fig.29 Vcc voltage at startup

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(9) Minus voltage of each pin

In some cases, the voltage oscillation of Vds just before MOSFET turns on is applied to the OUT pin through parasitic capacitors, etc. and minus voltage may be added to the OUT pin. If this minus voltage is large, the parasitic element inside the IC is activated, and the IC may malfunction.

If this minus voltage is expected to exceed -0.3V, Schottky barrier diode should be connected between the OUT pin and GND. With the forward voltage of the Schottky barrier diode, the minus voltage can be clamped.

For other pins as well, care should be taken so that minus voltage will not be applied in the same way.

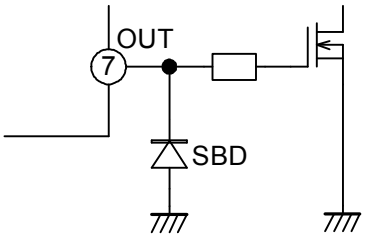

Fig.30 Protection circuit of OUT pin against the negative voltage

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12. Advice for design

(1) Advice in pattern designing

Main power parts such as MOSFET, inductor, and diode in the main switching circuit are operating with large voltage and current. For this reason, if the IC or wires of input signals are located close to these main power parts, malfunction may occur affected by noise generated there.
Special care should be taken to the following cases. (Bad examples)

- IC is placed under the main circuit parts such as inductor or just on the back side of the main circuit parts in case of a double-sided board. (Fig. 31)
- IC is placed just beside the inductor, MOSFET or diode. (Fig. 32)
- Signal wires are placed under the inductor or near MOSFET or diode. (Fig. 33)

If the PFC output is used for the load circuit (DC/DC converter, inverter, etc.), branch the output capacitor so that the respective GND patterns in the PFC and load circuit are not interfered by the switching current. (Fig. 34)

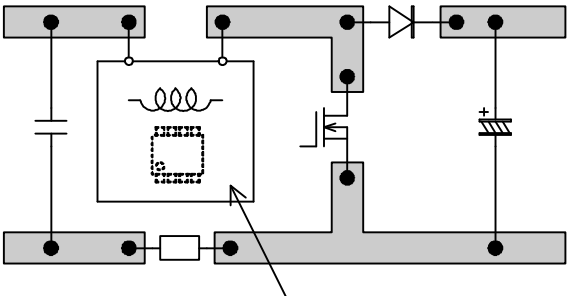

Fig.31 Bad example (1)

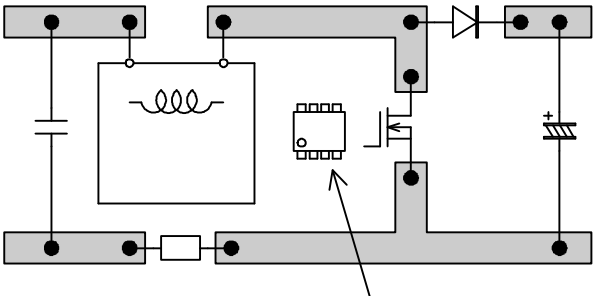

Fig.32 Bad example (2)

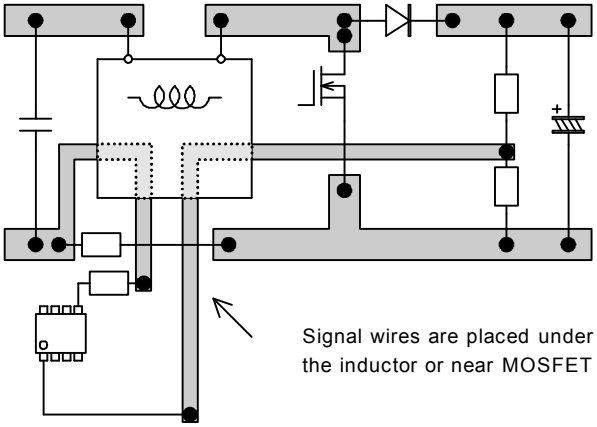

Fig.33 Bad example (3)

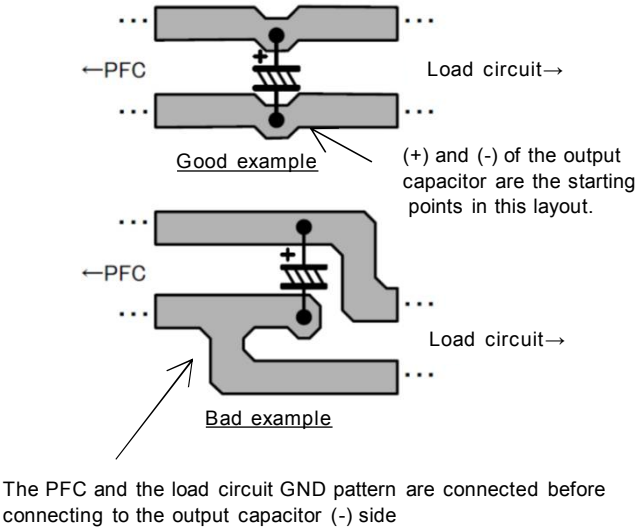

Fig.34 Pattern example of PFC- Load circuit

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(2)Example of GND wiring around IC

To minimize the influence of the main-circuit noise to the IC, separate the signal-system GND of the IC and its peripheral components from the PFC main-circuit GND, and connect them in single-point connection near the current detection resistor Rs. (Fig. 35)

The wiring between the CS pin and Rs and between Rs and GND must be as short as possible because the voltage level of the CS signal is low and so easily influenced by noise.

Set the VCC-GND capacitor immediately near the IC. If the capacitor is set far away from the IC, its effects are reduced. The capacitor between the input pin and the GND around the IC must be set immediately near the IC. If the capacitor is set far away from the IC, the IC may be influenced by noise because the capacitor also remove noise.

Notes）

Wiring is exemplified for you to understand how to connect the GND line.

Noise and incidental erratic operations differ from one instrument to another. Adopting any wiring exemplified in Fig. 36 will not necessarily guarantee normal operations of your instruments.

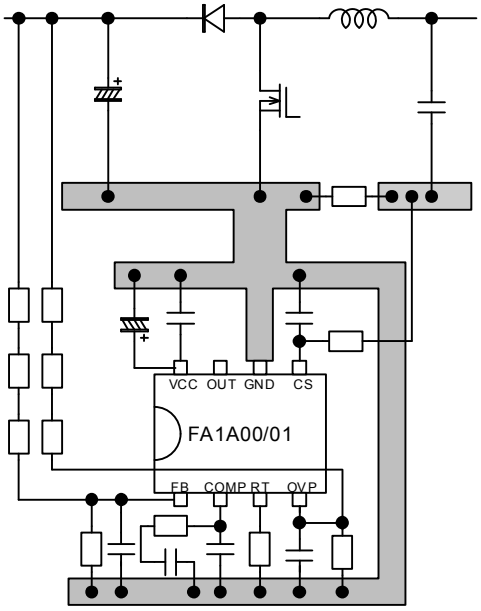

Fig.35 Good example of GND wiring around IC

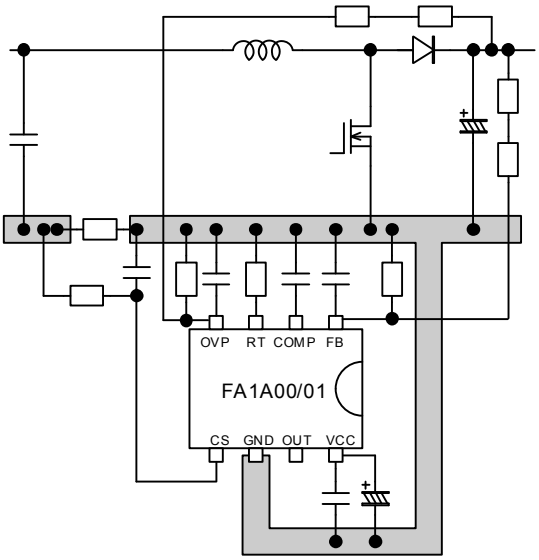

Fig.36 Bad example of GND wiring around IC

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(3) Cautions in use about pin noise

When the single-pulse noise is input each pin of IC, IC may malfunction following below. Please confirm that neither the instable operation nor the malfunction occurs by noise and use this IC

A noise input within the absolute maximum ratings

Condition	Pin	malfunction in fear	Input regulations	Cautions in design
Start Up	CS	It may not turn on if input voltage less than threshold voltage	Do input voltage more than threshold voltage	Design the PCB pattern to offset current is not generated in the inductor current sensing line
Input noise (within absolute maximum ratings)	FB	Switching may stop when noise is over OVP level	Input signal is only for feedback voltage of output voltage	Connect capacitor near pin
		IC may become standby mode when noise is under short detection level (after standby mode cancellation become restart)		
		Offset occurs in output voltage and output voltage rises or falls by a noise		
		Output voltage may fall when enter the dynamic OVP domain by a noise		
	COMP	On width may become not constant by load, output may change heavily by a noise	Cancel noise	Confirm sufficiently phase compensation constant
		Switching may become when noise is over threshold voltage		
		Switching may stop when noise is under threshold voltage		
	RT	On width may become not constant by load, output changes heavily by a noise	Cancel noise	Care the pattern of PCB
		Restriction of maximum on time may not work when voltage is higher than pin voltage (On width may change when voltage is higher than pin voltage)		
		On width and restriction may change when voltage is lower than pin voltage		
	OVP	Switching may stop when noise is over OVP level	Cancel noise	Connect capacitor near pin
	CS	Turn-on occurs unintentional timing, Mos/Diode heat and switching noise may become bigger by a noise	Cancel noise	Connect capacitor near pin
		It may not turn on when the time over turn-on threshold is less than delay time	Although Inductor and Mos capacitance is resonant, input voltage more than threshold over delay time	Connect capacitor near pin
		Frequency reduction function may not work when noise frequency is faster than maximum frequency of setting	Cancel noise	Connect capacitor near pin
	GND	Reference voltage changes, IC may not behave normally	Cancel noise	Ground wiring should be a wide wiring
	OUT	The output may fall not to be able to drive Mos normally when signals more than the ability of the driver are input	Cancel noise	–
	VCC	IC may stop when noise under UVLO is input	Don't input noise under UVLO when operating	Connect capacitor near pin
Input minus voltage (less than absolute maximum voltage)	FB	A parasitism element works, and the malfunction such as IC stop may occur	Don't input minus voltage less than maximum absolute voltage	–
	COMP			
	RT			
	OVP			
	CS	IC may be destroyed		Please put a Diode with a current sense resistor in parallel
	OUT	IC may be destroyed		-
	VCC	A parasitism element works, and the malfunction such as IC stop may occur		-
Input plus voltage (more than absolute maximum voltage)	FB	IC may be destroyed	Don't input plus voltage more than maximum absolute voltage	-
	COMP			
	RT			
	OVP			
	CS	GND level may be changed		
	OUT	IC may be destroyed		
	VCC			

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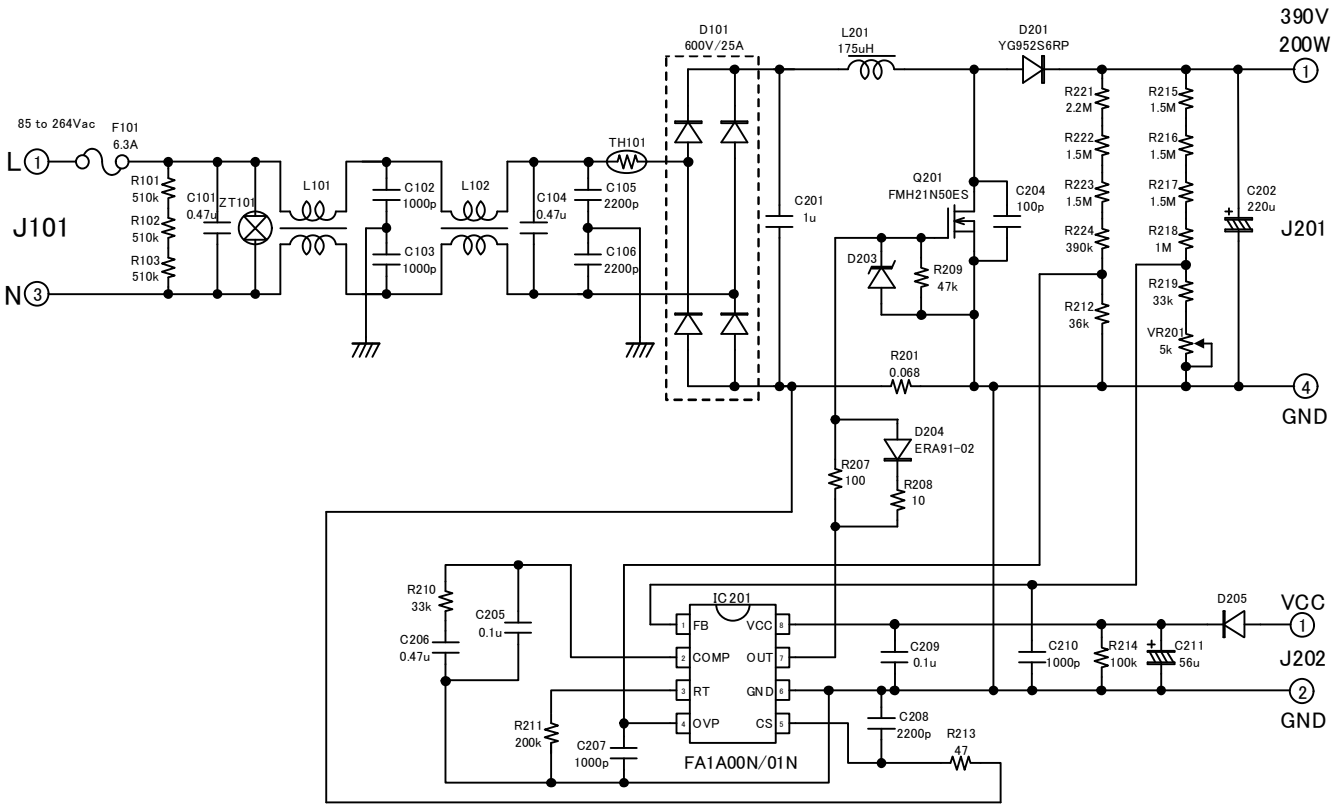
13. Example of application circuit



Note) This application circuit is a reference material for describing typical usage of this IC, and does not guarantee the operation or characteristics of the IC.

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